AMENDMENTS TO THE CLAIMS

Claims 1-26 (Canceled).

27. (Previously presented) An array of resistance variable memory cells in an integrated circuit, at least one memory cell comprising a pillar of stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode layer, a chalcogenide glass layer having metal ions diffused therein and being capable of changing resistance under the influence of an applied voltage, and a second electrode layer, each layer having [[a]] lateral edges, the lateral edges of each layer approximately vertically aligned with [[a]] lateral ~~edge~~ edges of each other layer.

28. (Previously presented) The array of Claim 27, further comprising insulating material in the regions between the pillars.

29. (Original) The array of Claim 28, wherein the insulating material comprises silicon oxide.

30. (Original) The array of Claim 29, wherein the silicon oxide comprises tetraethylorthosilicate (TEOS).

31. (Previously presented) The array of Claim 29, wherein the insulating material further comprises a silicon nitride layer below the silicon oxide that conforms to the pillars and to the substrate.

32. (Original) The array of Claim 31, wherein the silicon nitride layer is between 5 nm and 50 nm thick.

Claims 33-48 (Canceled).

49. (Previously presented) The array of Claim 27, wherein the metal ions comprise silver ions.

50. (Previously presented) The array of Claim 27, wherein at least one of the first and second electrodes is tungsten.